

## IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~striketrough~~.

[0022] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawings of which:

FIG.1A is a plan figure schematically illustrating a TFT in which the number of fatal crystal grain boundaries, for the size of equal crystal grains  $G_s$ , and the dimension of active channels  $L \times W$ , is 2;

FIG. 1B is a plan figure schematically illustrating a TFT in which the number of fatal crystal grain boundaries is 3;

FIG. 2A and FIG. 2B are plan figures schematically illustrating active channels of TFTs including silicon grains having a large grain size formed by the SLS crystallization method ;

FIG. 3A to FIG. 3C are plan figures schematically illustrating active channels of TFTs fabricated according to other related art;

FIG. 4A is a drawing indicating that "primary" crystal grain boundaries in active channel regions are arranged perpendicularly to the direction of current flowing from source to drain, and FIG. 4B is a drawing showing a  $V_{th}$  curve measured according to a position of a TFT in a substrate fabricated according to the arrangement of FIG. 4A; and

FIG. 5A is a drawing indicating that "primary" crystal grain boundaries in active channel regions are arranged parallel to the direction of current flowing from source to drain, and FIG. 5B is a drawing showing a  $V_{th}$  curve measured according to a position of a TFT in a substrate fabricated according to the arrangement of FIG. 5A.

FIG. 6 is a drawing illustrating a display device having a display region and a driving region and a plurality of thin film transistors.

Please add new paragraph [0040] and renumber old paragraph [0040] as paragraph [0041].

[0040] FIG. 6 is a drawing illustrating a display device. The display device includes a substrate 120, a display region 121 and driving regions 123. The display region 121 includes a regular array of pixels 122, each including a TFT pixel controller. Each pixel controller can be individually addressed by the drivers 123.